Abstracted Microarchitecture: Example Core i7 Haswell (2013) and Sandybridge (2011)

Throughput (tp) is measured in doubles/cycle. For example: 4 (2). Numbers are for loading into registers.

Latency (lat) is measured in cycles

1 double floating point (FP) = 8 bytes

fma = fused multiply-add

Rectangles not to scale

Haswell

Sandy Bridge

**double FP:**

max scalar tp:
- 2 fmas/cycle =
- 2 (1) adds/cycle and
- 2 (1) mults/cycle

max vector tp (AVX):
- 2 vfmas/cycle = 8 fmas/cycle =
- 8 (4) adds/cycle and
- 8 (4) mults/cycle

**ISA**

**1 Core**

(see page for details)

Core i7-4770 Haswell:
4 cores, 8 threads
3.4 GHz
(3.9 GHz max turbo freq)
2 DDR3 channels 1600 MHz

**Memory hierarchy:**
- Registers
- L1 cache
- L2 cache
- L3 cache
- Main memory
- Hard disk

**Source:** Intel manual (chapter 2), http://www.7-cpu.com/cpu/Haswell.html